WHAT IS CLAIMED IS:

1. A semiconductor device provided at least with a semiconductor layer including source and drain areas of a first conductive type and of a high impurity concentration and a channel area positioned between said source and drain areas, an insulation layer covering at least said channel area, and a gate electrode positioned close to said insulation layer, wherein said channel area at least comprises a first channel area of a low resistance, positioned close to said insulation layer and having a second conductive type opposite to said first conductive type, and a second channel area of a high resistance, having said first conductive type and positioned adjacent to said first channel area.

2. A semiconductor device according to claim 1, further comprising a third channel area of the second conductive type, positioned adjacent to said second channel area.

3. A semiconductor device according to claim 1, wherein said second channel area is depleted at least when the voltage applied to the gate electrode is zero.

4. A semiconductor device according to claim

1, wherein the thickness of said first channel area is larger than the mean free path of the drifting carriers.

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5. A semiconductor device according to claim 1, wherein said semiconductor layer is formed on an insulating member.

6. A semiconductor device according to claim 5, further comprising a third channel area of the second conductive type, positioned adjacent to said second channel area.

7. A semiconductor device according to claim 5, wherein said second channel area is depleted at least when the voltage applied to the gate electrode is zero.

8. A semiconductor device according to claim 5, wherein the thickness of said first channel area is larger than the mean free path of the drifting carriers.

9. A semiconductor device according to claim 1, further comprising a third channel area of the second conductive type, positioned adjacent to said second channel area.

10. A semiconductor device according to claim 9, constituting an integrated circuit including a MIS transistor in which said second channel area is depleted at least when the voltage applied to the gate electrode is zero.

11. A secmiconductor device according to claim 9, constituting an integrated circuit including a MIS transistor comprising a fourth channel area of the first conductive type, positioned between the first and second channel areas.

12. A semiconductor device according to claim 9, constituting an integrated circuit including a MIS transistor in which the potential distribution in the channel area is higher at the surface in the functional state under a gate voltage application, whereby the carriers drift in an area deeper than the mean free path of said carriers from the interface.

13. A semiconductor device according to claim 10 wherein said MIS transistor is an enhancement MIS transistor.

14. A semiconductor device according to claim 1, wherein the impurity concentration of said source and drain areas is within a range of 10^{18} to 10^{21} cm^{-3}.

15. A semiconductor device according to claim 1, wherein the impurity concentration of said first channel area is within a range of 10^{15} to 10^{19} cm^{-3}.

16. A semiconductor device according to claim 1, wherein the impurity concentration of said second channel area is 1×10^{17} cm^{-3} or lower.

17. A semiconductor device according to claim 1, wherein said first conductive type is n-type.

18. A semiconductor device according to claim 1, wherein said second conductive type is p-type.

19. A semiconductor device according to claim 9, wherein the impurity concentration of said third channel area is within a range of 10^{14} to 10^{18} cm^{-3}.